	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L2	193	leadless and tape and (flipchip or flip adj chip)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/09 11:11

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L5	1413453	concav$6 or curv$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
2	BRS	L6	1815	half-etch$6 or (half adj etch$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
3	BRS	L7	649797	pad$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
4	IS&R	L9	1944	(438/614).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
5	IS&R	L10	1544	(257/690).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	IS&R	L11	1624	(257/786).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
7	IS&R	L12	1169	(257/750).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
8	BRS	L4	215	leadless and tape and (flipchip or flip adj chip)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 15:30
9	BRS	L8	20	(half-etch$6 or (half adj etch$6)) same (concav$6 or curv$6) same pad$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:03
10	BRS	L13	3719	half near4 etch$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:04

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L14	426869	pad	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:04
12	BRS	L15	305	13 same 14	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:05
13	BRS	L16	280	15 and (chip or die or dice or device)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:05
14	BRS	L17	18900889	(@ad<20000128) or (@rlad<20000128)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:07
15	BRS	L18	104	16 and 17	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/21 16:07

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	2285	(438/612).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 13:49
2	IS&R	L40	777	(438/124).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 14:04
3	IS&R	L41	12	(("6201292") or ("6198171") or ("5900676") or ("6187614") or ("6208023")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 14:08
4	IS&R	L43	1119	(438/127).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 15:00
5	IS&R	L42	760	(438/126).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 15:00

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	IS&R	L44	326	(438/617).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 15:12
7	IS&R	L47	74	(438/438).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/22 15:30
8	BRS	L48	4	("5200362" | "6001671" | "6093584" | "6159770").PN.	USPAT	2004/10/22 15:31
9	BRS	L49	32	6159770.URPN.	USPAT	2004/10/22 15:32

US-PAT-NO: **6072239**

DOCUMENT-IDENTIFIER: US 6072239 A

TITLE: Device having resin package with projections

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US Patent No. - PN (1):
6072239

Brief Summary Text - BSTX (3):
The present invention generally relates to devices having a resin package such as semiconductor devices, and more particularly to a resin-sealed semiconductor device of a **leadless** surface mounting type directed to high-density mounting. Further, the present invention is concerned with a method of producing such a semiconductor device.

Brief Summary Text - BSTX (33):
The device may be configured so that the first resin portion comprises a resin **tape** (183).

Brief Summary Text - BSTX (51):
The method may be configured so that it further comprises a step of providing a **tape** member to the molded resin packages before the step (e) is executed.

Drawing Description Text - DRTX (58):
FIG. 52A is a plan view showing a **tape** arranging step of the method of the semiconductor device according to the tenth embodiment of the present

invention;

Drawing Description Text - DRTX (59):
FIG. 52B is a side view of the **tape** arranging step of the method of the semiconductor device according to the tenth embodiment of the present invention;

Drawing Description Text - DRTX (66):
FIG. 56 is a plan view observed when the **tape** arranging step for the lead frame shown in FIG. 55A is completed;

Detailed Description Text - DETX (111):
Subsequent to the sealing step, a **tape** arranging step is carried out. In this step, as shown in FIGS. 52A and 52B, a **tape** member 133 is arranged on the tops of the resin packages 112. The **tape** member 133 has a surface coated with an adhesive, and a base **tape** which cannot be damaged by an

Detailed Description Text - DETX (112):
etchant used in a separating step which will be carried out later. The **tape** member 133 joins the resin packages 112 together, so that the resin packages 112 are supported by the **tape** member 133 even when the resin packages 112 are separated from the lead frame 120.

Detailed Description Text - DETX (113):
The **tape** member 133 can be arranged at an appropriate time before the resin packages 112 are formed. For example, the **tape** member 133 can be arranged within the die prior to the sealing step. In this case, when the resin packages 112 are formed, the resin packages 112 are joined together by the **tape** member 133.

Detailed Description Text - DETX (114):

Following the **tape** arranging step, a separating step is carried out in order to separate the resin packages 112 from the lead frame 120. FIG. 53 shows the separating step, in which the lead frame 120 is placed in the etchant and is thus dissolved. It is required that the etchant used in the separating step can dissolve the lead frame 120 only and does not dissolve the metallic films 113C. When the lead frame 120 is completely dissolved, the resin packages 112 are separated from the lead frame 120. The above separating step makes it possible to certainly and easily separate the resin packages 112 from the lead frame 120.

Detailed Description Text - DETX (115):

FIGS. 54A and 54B show the semiconductor devices 110 when the separating step is completed. At this time, the semiconductor devices 110 are supported by the **tape** member 133. Hence, it is easy to handle the chips 110 after the separation step. When the **tape** member 133 is wound and shipped, it is possible to automatically mount the semiconductor devices 110 to a circuit board, as in the case of chips or electronic components.

Detailed Description Text - DETX (118):

FIG. 55A shows a first variation of the sealing step. In the above-mentioned method, the resin packages 112 are joined by the on-gate resin portions as has been described with reference to FIG. 49. The on-gate resin portions are removed as shown in FIGS. 51A and 51B, and the **tape** member 133 is arranged as shown in FIGS. 52A and 52B. As has been described, the **tape** member 133 is used to maintain the separated resin packages 112 in the respective

original positions.

Detailed Description Text - DETX (119):
In the first variation, the on-gate resin portions and the resin 129 remaining in the runner 131 are used, instead of the **tape** member 133, as resin joint members joining the resin packages 112 together. Hereinafter, such resin joint members are referred to as a runner frame 134. Hence, it is possible to efficiently utilize the on-gate resin portions and the resin 129 remaining in the runner 131. The runner frame 134 should be removed when shipping the semiconductor devices 110. In this case, before shipping, the **tape** member 133 is provided as shown in FIG. 56, and the runner frame 134 is removed (resin joint member removing step).

Detailed Description Text - DETX (120):
It is possible to prevent the **tape** member 133 from being damaged in the separating step and a step of testing the semiconductor devices 110 by providing the **tape** member 133 before shipping. This is advantageous when the semiconductor devices 110 are shipped in the state in which the devices 110 are shipped.

Detailed Description Text - DETX (124):
FIGS. 57A and 57B show the lead frame 120 when the sealing step is completed in the fourth variation. As shown in these figures, the resin packages 112 are joined like a plate-shaped chocolate. There are grooves 135 at the boundaries of the adjacent resin packages 112. Hence, it is possible to keep the original positions of the resin packages 112 without the **tape** member 133. The resin packages 112 can be separated from each other in the grooves 135, which

facilitate the separating step.

Detailed Description Text - DETX (165):
The semiconductor device 180 has a resin package 181 made up of an upper resin layer 182 and a lower resin layer 183, in which the lower resin layer 183 is formed by an insulation resin **tape**. Windows 184 are formed in given positions in the resin **tape** 183, and external electrode films 185 are formed to the lower surface (mounting surface) of the resin **tape** 183 so that the electrode films 185 cover the windows 184. The bonding wires 118 are bonded to the electrode films 185 through the windows 184.

Detailed Description Text - DETX (166):
The semiconductor device 180 has improved characteristics resulting from the two-layer package structure, and a cost reduction due to the resin **tape** 183 used instead of the lead frame 120 or 159.

Detailed Description Text - DETX (196):
An alternative separating step shown in FIG. 94 can be employed instead of the separating step shown in FIG. 53. An etching apparatus 260 shown in FIG. 94 includes a feed reel 261, an etching chamber 262, and a take-up reel 263. A plurality of lead frames 220 to which the resin packages 212 are provided are attached to a **tape** member 233, which is wound on the feed reel 261. Nozzles 264 for injecting etchant are provided in the etching chamber 262. The **tape** member 233 is fed from the feed reel 261 and is supplied to the etching chamber 262, in which the lead frame 262 facing the nozzles 264 is etched. By the etching process, the lead frame 220 is dissolved except for the metallic films 231C. Hence, the resin packages 212 are separated from the lead frame 220.

Detailed Description Text - DETX (197):
The **tape** member 233 is formed of a material not affected by the etchant, so that the resin packages 212 are supported by the **tape** member 233 after the lead frame 220 is dissolved. The **tape** member 233 by which the packages 212 are supported goes out of the etching chamber 262, and is wound by the take-up reel 263. By using the above etching apparatus, it is possible to automatically separate the packages 212 from the lead frame 220.

Detailed Description Text - DETX (211):
FIGS. 102A through 102E show yet another separating step. FIG. 102A shows that the resin packages 212 are supported by the lead frame 220. The runner frames 234 are not formed. As shown in FIG. 102B, a sheet member 2105 is provided so as to cover the resin packages 212 after the sealing step is carried out and before the lead frame 220 is removed. The sheet member 2105 is not supplied with any adhesive, while the aforementioned **tape** member 233 is supplied with an adhesive.

Detailed Description Text - DETX (266):
Thereafter, a **tape** arrangement step is carried out in the same manner as that already described with reference to FIGS. 52A and 52B.

Detailed Description Text - DETX (267):
Then, a separating (etching) step which corresponds to the separating step shown in aforementioned FIG. 53 is carried out, as shown in FIG. 130 in which a reference number 333 indicates a **tape** member which corresponds to the **tape** member 133 shown in aforementioned FIG. 53.

Detailed Description Text - DETX (268):
The semiconductor devices 310 observed after the lead frame 320 are supported by the **tape** member 333, as shown in aforementioned FIGS. 54A and 54B.

Detailed Description Text - DETX (281):
FIG. 135 shows a semiconductor device 310E according to a twenty-third embodiment of the present invention. In FIG. 135, parts that are the same as those shown in the previously described figures are given the same reference numbers. The semiconductor device 310E does not use bonding wires which connect the electrode pads 312 and the metallic films 315. Instead of such bonding wires, bumps 342 are used to electrically connect the electrode pads 312 and the metallic films 315. The use of the bumps 342 makes it possible to reduce the height of the semiconductor device 310E and to provide a thinner package. The bumps 342 can be provided by **flip-chip** bonding, which is faster than wire bonding. Hence, it is possible to reduce the time necessary to connect the electrode pads 312 and the metallic films 315 together.

Detailed Description Text - DETX (282):
The semiconductor device 310E can be produced in almost the same manner as that of producing the semiconductor device 310 except for the following. When the chip 311 is mounted on the lead frame 320, the **flip-chip** bonding is carried out so that the electrode pads 312 are connected to the metallic films 315 via the bumps 342, which can be preformed to either the electrode pads 312 or the metallic films 315.

Detailed Description Text - DETX (283):
As shown in FIG. 136A showing a semiconductor device

310F, the bonding wires
313 of the semiconductor device 310B shown in FIG. 132 can be replaced by bumps
342. The **flip-chip** bonding is carried out for the leading portions 3151 of the
metallic films 315. It is possible to increase the pitch at which the metallic
films 315 provided on the resin projections 318 are arranged.

Detailed Description Text - DETX (285):
bumps 342 are provided so as to engage the recess portions 343 by the
flip-chip bonding. The use of the recess portions 343 facilitates the
positioning of the bumps 342.

Detailed Description Text - DETX (291):
FIG. 140 shows a semiconductor device 310L, which has an insulating member
347 which is flush with the bottom surface of the resin package 314. The
insulating member 347 can be formed of a **tape,** an adhesive or the like. The
insulating member 347 is provided taking into account a possibility that it may
be difficult for the mold resin to enter the gap between the chip 311 and the
lead frame 320 in the resin molding step because the above gap is very small.
In this case, the sealing may be defective. The insulating member 347 provided
beforehand to the element forming surface of the chip 311 prevents occurrence
of defective sealing even if the gap is completely full of the mold resin. The
insulating member 347 can be provided to either the chip 311 or the lead frame
320 before the **flip-chip** bonding is carried out.